

Amendments To The Claims:

Please amend the claims as follows:

Please cancel claims 1-21.

Please add the following new claims 22-57 as follows:

- 22 (New). A method of writing information to a memory device comprising:
examining a present word to be written, said present word having N bits, each of said bits having a first value and a second value;
comparing said present word to a previous word having N bits and determining a number of transitions of bits from said first value in said previous word to said second value in said present word;
inverting said present word when said number of transitions is greater than or equal to a threshold;
writing said present word to said memory device.
- 23 (New). The method of claim 22 wherein said threshold is $N/2$.
- 24 (New). The method of claim 22 wherein said first value is a low value.
- 25 (New). The method of claim 22 wherein said first value is a high value.
- 26 (New). The method of claim 22 wherein said second value is a low value when said first value is said high value.
- 27 (New). The method of claim 22 wherein said second value is a high value when said first value is said low value.

- 28 (New). The method of claim 22 further including sending a data inversion mask (DIM) bit with said present word to indicate when said present word is inverted.
- 29 (New). The method of claim 22 wherein said memory device comprises a DRAM.
- 30 (New). The method of claim 22 wherein said word represents data.
- 31 (New). The method of claim 22 wherein said word represents graphical data.
- 32 (New). The method of claim 22 wherein said information represents one or more commands.
- 33 (New). The method of claim 22 wherein said information represents address information.
- 34 (New). A method of reading information from a memory device comprising:
examining a present word in said device to be read, said word having bits having a first value or a second value;
comparing said present word to a previous word and determining a number of transitions of bits having said first value in said previous word to bits having said second value in said present word;
inverting said present word when said number of transitions is greater than or equal to a threshold;
reading said present word from said device.

35 (New). The method of claim 34 wherein said threshold is $N/2$ where said present word has N bits.

36 (New). The method of claim 34 wherein said first value is a low value.

37 (New). The method of claim 34 wherein said first value is a high value.

38 (New). The method of claim 34 wherein said second value is a low value when said first value is said high value.

39 (New). The method of claim 34 wherein said second value is a high value when said first value is said low value.

40 (New). The method of claim 34 further including sending a data inversion mask (DIM) bit with said present word to indicate when said present word has been inverted.

41 (New). The method of claim 40 wherein said DIM bit is sent on an existing pin on said memory device.

42 (New). The method of claim 41 wherein said existing pin is a data mask (DM) pin.

43 (New). The method of claim 34 wherein said previous word is presumed to have all low values when said previous word is unknown.

44 (New). The method of claim 34 wherein said previous word is presumed to have all high values when said previous word is unknown.

45 (New). The method of claim 34 wherein said present word is not inverted when said previous word is unknown.

46 (New) . The method of claim 34 wherein said present word is latched and used as said previous word in a subsequent read operation.

47 (New). The method of claim 34 wherein said information comprises data.

48 (New). The method of claim 34 wherein said information comprises graphical data.

49 (New). The method of claim 34 wherein said information comprises one or more commands.

50 (New). The method of claim 34 wherein said information comprises address information.

51 (New). A memory device comprising:

a data array having an I/O pin; and

a data inversion mask generator.

52 (New). The memory device of claim 51 wherein said data inversion mask generator further comprises:

a first data register that stores a first plurality of bytes;

a second data register that stores a second plurality of bytes; and

a comparator.

53 (New). The memory device of claim 51 further comprising:
an exclusive-OR gate with a plurality of bits of data from said I/O pin as a first input and a data inversion mask bit as a second input; and
a data array connected to output of said exclusive-OR gate.

54 (New). A memory device comprising:
a read data bus connected to an input of a flip-flop, a first input of a comparator, and a first input of a NOR gate;
a load signal connected to an enable input of said flip-flop;
an output of said flip-flop connected to a first input of an OR gate;
a DC optimizing signal connected to a second input of said OR gate;
an output of said OR gate connected to a second input of said comparator;
an output of said comparator connected to a data inversion mask bit and to a second input of said NOR gate; and
an output of said NOR gate connected to an I/O pin.

55 (New). A memory device comprising:
a DRAM, wherein said DRAM comprises:
a first data bank from which data is read;
a second data bank from which data is read;
a memory controller combining an output bus from said first data bank with an output bus from second data bank to form a combined bus;
said combined bus connected to a first input of a microprocessor;
a data inversion mask bit from said first data bank connected to a first input of an exclusive OR gate;
a data inversion mask bit from said second data bank connected to a second input of said exclusive OR gate; and

an output of said exclusive OR gate connected to a second input of said microprocessor.

56 (New). A memory device comprising:

a write data bus connected to an input of a first flip-flop;

a data inversion mask connected to an input of a second flip-flop;

a write clock signal connected to an enable input of each of said first flip-flop and said second flip-flop;

an output of said first flip-flop connected to a first input of a NOR gate;

an output of said second flip-flop connected to a second input of said NOR gate; and

an output of said NOR gate connected to an I/O pin.